IN THE CLAIMS

1. (Original) A method for processing an information based on a sequence of instructions, said method comprising the steps of:

a) detecting a repeated sub-sequence in said sequence of instructions;

b) providing an index information indicating the repetition frequency of said repeated sub-sequence; and

c) determining an allocation between a processing resource and said repeated sub-sequence based on said index information.

2. (Original) A method according to claim 1, further comprising the step of generating an instruction containing said index information, and adding said instruction to said sequence of instructions.

3. (Currently amended) A method according to claim 1 ~~or 2~~, wherein said index information comprises an integer number set in proportion with a ranking of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences.

4. (Original) A method according to claim 3, wherein said allocation is determined by comparing said integer number with the number of available processing resources (20-2n).

5. (Original) A method according to claim 4, wherein all repeated sub-sequences for which said integer number is smaller than said number of available processing resources are allocated to a selected processing resource.

6. (Currently amended) A method according to ~~any one of the preceding claims~~claim 1, wherein said index information comprises an information indicating the number of instructions in said repeated sub-sequence.

7. (Currently amended) A method according to ~~any of the preceding claims~~claim 1, further comprising the step of generating an instruction for deleting said repeated sub-sequence, if said repeated sub-sequence is no longer detected for a predetermined time period, and resetting a processing unit to which said deleted repeated sub-sequence was allocated.

8. (Currently amended) A method according to ~~any one of the preceding claims~~claim 1, further comprising the step of generating an instruction for specifying processing registers used by said repeated sub-sequence, and using said instruction for locking said specified processing registers.

9. (Original) A method according to claim 2, further comprising the step of activating a processing resource (20-2n) when said instruction containing said index information indicates that the corresponding repeated sub-sequence has already been allocated to said processing resource.

10. (Original) A method according to claim 9, wherein said activating step comprises the step of programming said processing resource according to said corresponding repeated sub-sequence, or uploading said corresponding repeated sub-sequence to a memory of said processing resource.

11. (Currently amended) A method according to ~~any one of the preceding claims~~claim 1, further comprising the step of signalling the presence of external processing units (20-2n) to a central processing unit (10), and counting the number of available external processing units based on said signalling.

12. (Original) An apparatus for processing an information based on a sequence of instructions, said apparatus comprising:

a) detecting means (30) for detecting a repeated sub-sequence in said sequence of instructions, and for providing an index information indicating the repetition frequency of said repeated sub-sequence; and

b) resource control means (10) for allocating said repeated sub-sequence to a processing resource based on said index information.

13. (Original) An apparatus according to claim 12, further comprising connecting means for connecting at least one external processing unit (20-2n) to which said repeated sub-sequence can be allocated.

14. (Original) An apparatus according to claim 13, further comprising a memory table (40) for storing an allocation information indicating an allocation between said at least one external processing unit (20-2n) and corresponding repeated sub-sequences.

15. (Currently amended) An apparatus according to claim 13 ~~or 14~~, wherein said apparatus is a digital signal processor (10) and said at least one external processing units (20-2n) are processor cores and/or configurable logic blocks.

16. (Currently amended) An apparatus according to ~~any one of claims 13 to 15~~claim 13, further comprising means for determining the number of said at least one external processing units (20-2n) connected to said connecting means.

17. (Currently amended) An apparatus according to ~~any one of claims 13 to 16~~claim 13, further comprising mapping means for mapping said repeated sub-sequence to an available one of said at least one external processing unit (20-2n) based on said index information.

18. (Original) A compiler for providing an output sequence of instructions to be used for processing an information, said compiler being arranged to detect a repeated sub-sequence in said output sequence of instructions and to provide an index information indicating the repetition frequency of said repeated sub-sequence.

19. (Original) A compiler according to claim 18, wherein said compiler (30) is arranged to add to said repeated sub-sequence an instruction specifying said index information.

20. (Original) A compiler according to claim 19, wherein said additional instruction is added so as to precede said repeated sub-sequence.

21. (Currently amended) A compiler according to ~~any one of claims 18 to 20~~claim 18, wherein said compiler (30) is arranged to add to said output sequence an instruction for indicating that said repeated sub-sequence is not used anymore.

22. (Currently amended) A compiler according to ~~any one of claims 18 to 21~~claim 18, wherein said compiler (30) is arranged to add to said output sequence an instruction for allocating at least one processing register means until said repeated sub-sequence is finished.

23. (Currently amended) A compiler according to ~~any one of claims 18 to 21~~claim 18, wherein said compiler (30) is arranged to determine a ranking of repeated sub-sequences based on their repetition rate.